MAX17575

4.5V–60V, 1.5A, High-Efficiency, Synchronous Step-Down DC-DC Converter with Internal Compensation

General Description

The MAX17575 high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operates over a 4.5V to 60V input. The converter can deliver up to 1.5A and generates output voltages from 0.9V up to 0.9 x V_{IN}. The feedback (FB) voltage is accurate to within ±1.2% over -40°C to +125°C. The MAX17575 uses peak current-mode control.

The device is available in a 12-pin (3mm × 3mm) TDFN package. Simulation models are available.

Applications

- Industrial Control Power Supplies
- General-Purpose Point-of-Load
- Distributed Supply Regulation
- Base Station Power Supplies
- Wall Transformer Regulation
- High-Voltage, Single-Board Systems

Benefits and Features

- Reduces External Components and Total Cost
  - No Schottky-Synchronous Operation
  - Internal Compensation for Any Output Voltage
  - All-Ceramic Capacitors, Compact Layout
- Reduces Number of DC-DC Regulators to Stock
  - Wide 4.5V to 60V Input
  - Adjustable 0.9V to 0.9 × V_{IN} Output
  - Continuous 1.5A Current Over Temperature
  - 400kHz to 2.2MHz Adjustable Switching Frequency with External Synchronization
- Reduces Power Dissipation
  - Peak Efficiency > 92%
  - Auxiliary Bootstrap LDO for Improved Efficiency
  - 4.65µA Shutdown Current
- Operates Reliably in Adverse Industrial Environments
  - Hiccup Mode Overload Protection
  - Adjustable Soft-Start
  - Built-In Output-Voltage Monitoring with $\overline{RESET}$
  - Programmable EN/UVLO Threshold
  - Monotonic Startup into Prebiased Load
  - Overtemperature Protection
  - High Industrial -40°C to +125°C Ambient Operating Temperature Range/-40°C to +150°C Junction Temperature Range

***Ordering Information* appears at end of data sheet.**

19-8785; Rev 1; 6/17

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Absolute Maximum Ratings (Note 1)

V_{IN} to PGND .....-0.3V to +65V
EN/UVLO to GND.....-0.3V to V_{IN} + 0.3V
$EXTV_{CC}$ to GND .....-0.3V to +26V
BST to PGND .....-0.3V to +70V
LX to PGND.....-0.3V to (V_{IN} + 0.3)V
BST to LX.....-0.3V to +6.5V
BST to V_{CC} .....-0.3V to +65V
$\overline{RESET}$, SS, RT/SYNC to GND.....-0.3V to +6.5V
PGND to GND.....-0.3V to +0.3V
FB to GND.....-0.3V to +1.5V

V_{CC} to PGND.....-0.3V to +6.5V
LX Total RMS Current .....±1.6A
Continuous Power Dissipation (T_A = +70°C)
(derate 24.4mW/°C above +70°C) (Multilayer board)..1951mW
Output Short-Circuit Duration.....Continuous
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Junction temperature greater than +125°C degrades operating lifetimes.

Package Information

PACKAGE TYPE: 12 TDFN	
Package Code	TD1233+1C
Outline Number	**21-0664**
Land Pattern Number	**90-0397**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	41°C/W
Junction to Case (θ_{JC})	8.5°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics

(V_{IN} = $V_{EN/UVLO}$ = 24V, R_{RT} = 40.2k, C_{VCC} = 4.7µF, V_{PGND} = V_{GND} = $EXTV_{CC}$ = 0, LX = SS = $\overline{RESET}$ = OPEN, V_{BST} to V_{LX} = 5V, V_{FB} = 1V, T_A = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})						
Input Voltage Range	V_{IN}		4.5		60	V
Input Shutdown Current	I_{IN-SH}	$V_{EN/UVLO}$ = 0V (shutdown mode)		4.65	7.25	µA
Input Quiescent Current	I_{Q_PWM}	Normal switching mode, f_{SW} = 500kHz, V_{FB} = 0.8V, $EXTV_{CC}$ = GND		5.2		mA
ENABLE/UVLO (EN)						
EN/UVLO Threshold	V_{ENR}	$V_{EN/UVLO}$ rising	1.19	1.215	1.26	V
	V_{ENF}	$V_{EN/UVLO}$ falling	1.068	1.09	1.131	V
EN/UVLO Input Leakage Current	I_{ENLKG}	$V_{EN/UVLO}$ = 1.25V, T_A = 25°C	-50		+50	nA
V_{CC} LDO						
V_{CC} Output-Voltage Range	V_{CC}	1mA ≤ I_{VCC} ≤ 15mA	4.75	5	5.25	V
		6V ≤ V_{IN} ≤ 60V; I_{VCC} = 1mA	4.75	5	5.25	V
V_{CC} Current Limit	$I_{VCC-MAX}$	V_{CC} = 4.3V, V_{IN} = 6.5V	25	54	100	mA
V_{CC} Dropout	V_{CC-DO}	V_{IN} = 4.5V , I_{VCC} = 15mA	4.15			V
V_{CC} UVLO	V_{CC-UVR}	Rising	4.05	4.2	4.3	V
	V_{CC-UVF}	Falling	3.65	3.8	3.9	V
EXT LDO						
$EXTV_{CC}$ Switchover Voltage		$EXTV_{CC}$ rising	4.56	4.7	4.84	V
		$EXTV_{CC}$ falling	4.3	4.45	4.6	V
$EXTV_{CC}$ Dropout	$EXTV_{CC-DO}$	$EXTV_{CC}$ = 4.75V , I_{EXTVCC} = 15mA			0.3	V
$EXTV_{CC}$ Current Limit	EXT V_{CCILIM}	V_{CC} = 4.5V, $EXTV_{CC}$ = 7V	26.5	60	100	mA
HIGH-SIDE MOSFET AND LOW-SIDE MOSFET DRIVER						
High-Side nMOS On-Resistance	R_{DS-ONH}	I_{LX} = 0.3A		330	620	mΩ
Low-Side nMOS On-Resistance	R_{DS-ONL}	I_{LX} = 0.3A		170	320	mΩ
LX Leakage Current (LX to PGND_)	ILX_{LKG}	V_{LX} = V_{IN}-1V; V_{LX} = V_{PGND} +1V; T_A = 25°C	-2		+2	µA
SOFT-START						
Soft-Start Current	I_{SS}	V_{SS} = 0.5 V	4.7	5	5.3	µA
FEEDBACK (FB)						
FB Regulation Voltage	V_{FB_REG}		0.889	0.9	0.911	V
FB Input Bias Current	I_{FB}	0 ≤ V_{FB} ≤ 1V, T_A = 25°C	-50		+50	nA

Electrical Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, R_{RT} = 40.2k, C_{VCC} = 4.7µF, V_{PGND} = V_{GND} = $EXTV_{CC}$ = 0, LX = SS = $\overline{RESET}$ = OPEN, V_{BST} to V_{LX} = 5V, V_{FB} = 1V, T_A = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

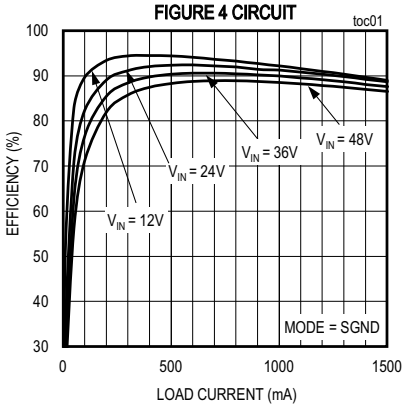
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT LIMIT						
Peak Current-Limit Threshold	$I_{PEAK-LIMIT}$		2.1	2.45	2.8	A
Runaway Current-Limit Threshold	$I_{RUNAWAY-LIMIT}$		2.3	2.75	3.1	A
Negative Current-Limit Threshold				1		A
RT/SYNC AND TIMINGS						
Switching Frequency	f_{SW}	R_{RT} = OPEN	430	490	550	kHz
		R_{RT} = 51.1kΩ	370	400	430	kHz
		R_{RT} = 40.2kΩ	475	500	525	kHz
		R_{RT} = 8.06kΩ	1950	2200	2450	kHz
V_{FB} Undervoltage Trip Level to Cause HICCUP	$V_{FB-HICF}$		0.56	0.58	0.65	V
HICCUP Timeout				32768		Cycles
Minimum On-Time	t_{ON_MIN}			60	80	ns
Minimum Off-Time	t_{OFF_MIN}		140	150	160	ns
LX Dead Time				5		ns
SYNC Frequency Capture Range		f_{SW} set by R_{RT}	1.1 x f_{SW}		1.4 x f_{SW}	
SYNC Pulse Width			50			ns
SYNC Threshold	V_{IH}		2.1			V
	V_{IL}				0.8	V
$\overline{RESET}$						
$\overline{RESET}$ Output Level Low		$I_{\overline{RESET}}$ = 10mA			400	mV
$\overline{RESET}$ Output Leakage Current		T_A = T_J = 25°C, $V_{\overline{RESET}}$ = 5.5V	-100		+100	nA
V_{OUT} Threshold for $\overline{RESET}$ Assertion	$V_{OUT-OKF}$	V_{FB} falling	90.5	92	94.6	%
V_{OUT} Threshold for $\overline{RESET}$ Deassertion	$V_{OUT-OKR}$	V_{FB} rising	93.8	95	97.8	%
$\overline{RESET}$ Delay After FB Reaches 95% Regulation				1024		Cycles
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold	T_{SHDNR}	Temp rising		165		°C
Thermal-Shutdown Hysteresis	T_{SHDNHY}			10		°C

Note 2: All limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization

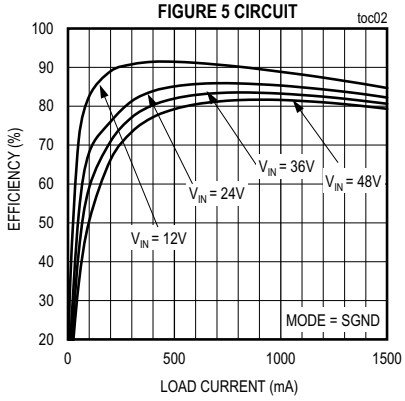
Typical Operating Characteristics

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{GND} = V_{PGND} = 0V, CV_{IN} = 2.2µF, C_{VCC} = 4.7µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

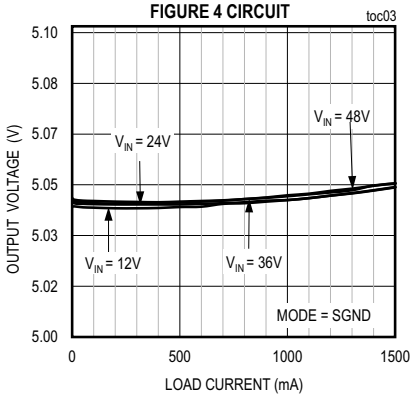
5V OUTPUT, PWM MODE, EFFICIENCY vs. LOAD CURRENT FIGURE 4 CIRCUIT



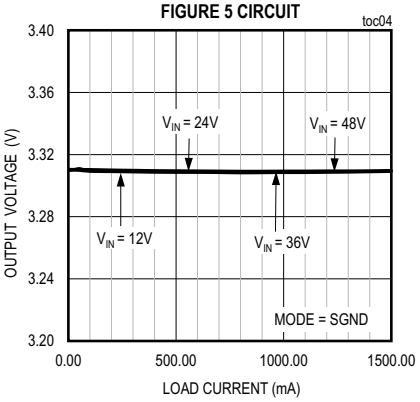
3.3V OUTPUT, PWM MODE, EFFICIENCY VS. LOAD CURRENT FIGURE 5 CIRCUIT



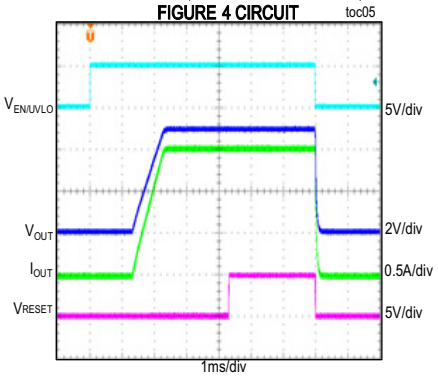
5V OUTPUT, PWM MODE, LOAD AND LINE REGULATION FIGURE 4 CIRCUIT



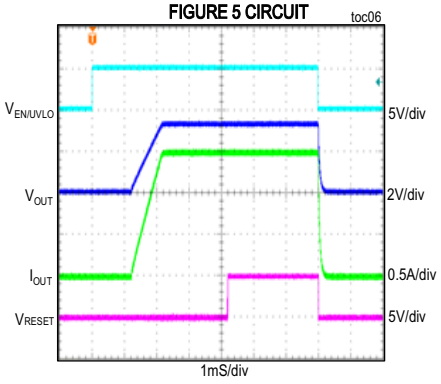
3.3V OUTPUT, PWM MODE, LOAD AND LINE REGULATION FIGURE 5 CIRCUIT



SOFT-START/SHUTDOWN FROM EN/UVLO, 5V OUTPUT, 1.5A LOAD CURRENT, FIGURE 4 CIRCUIT



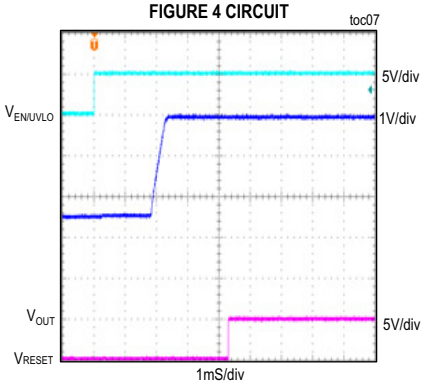
SOFT-START/SHUTDOWN FROM EN/UVLO, 3.3V OUTPUT, 1.5A LOAD CURRENT, FIGURE 5 CIRCUIT



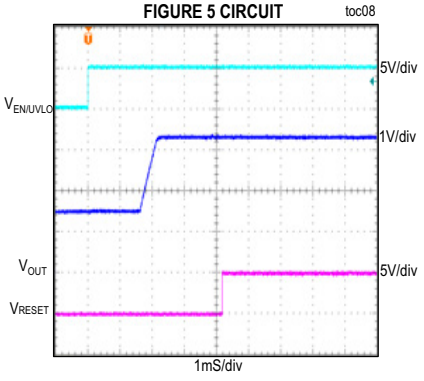
Typical Operating Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{GND} = V_{PGND} = 0V, CV_{IN} = 2.2µF, C_{VCC} = 4.7µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

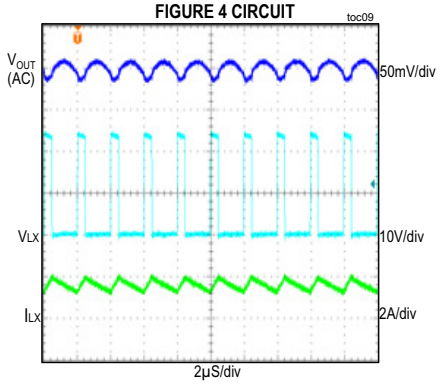
SOFT-START WITH 2.5V PREBIAS, 5V OUTPUT, PWM MODE, FIGURE 4 CIRCUIT



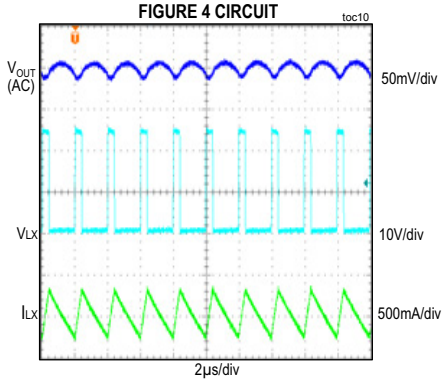
SOFT-START WITH 1.5V PREBIAS, 3.3V OUTPUT, PWM MODE, FIGURE 5 CIRCUIT



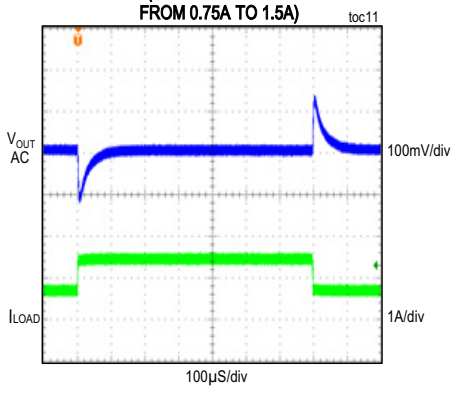
STEADY-STATE SWITCHING WAVEFORMS, 5V OUTPUT, 1.5A LOAD CURRENT, FIGURE 4 CIRCUIT



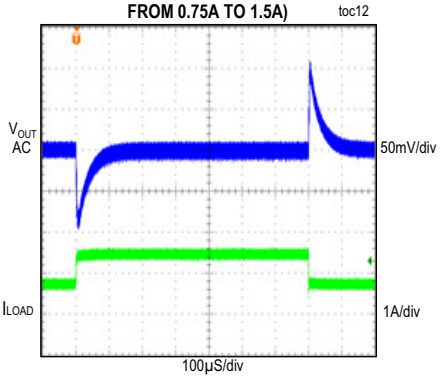
STEADY-STATE SWITCHING WAVEFORMS, 5V OUTPUT, NO LOAD CURRENT, FIGURE 4 CIRCUIT



5V OUTPUT, PWM MODE, FIGURE 4 CIRCUIT (LOAD CURRENT STEPPED FROM 0.75A TO 1.5A)



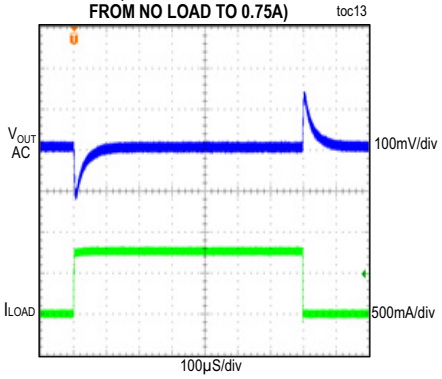
3.3V OUTPUT, PWM MODE, FIGURE 5 CIRCUIT (LOAD CURRENT STEPPED FROM 0.75A TO 1.5A)



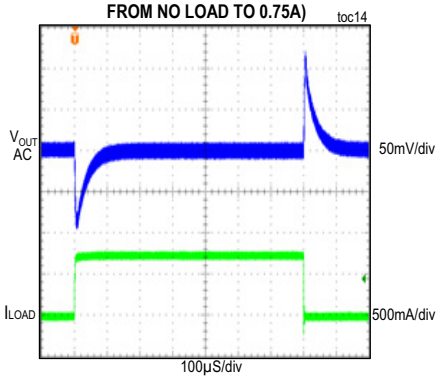
Typical Operating Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{GND} = V_{PGND} = 0V, CV_{IN} = 2.2µF, C_{VCC} = 4.7µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

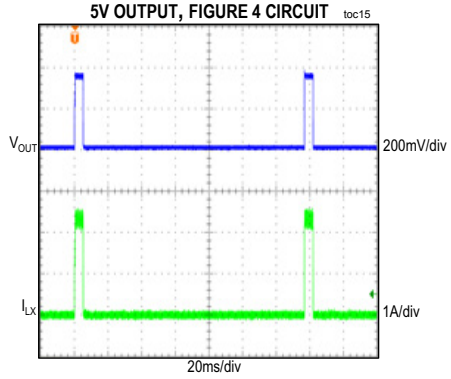
5V OUTPUT, PWM MODE, FIGURE 4 CIRCUIT (LOAD CURRENT STEPPED FROM NO LOAD TO 0.75A)



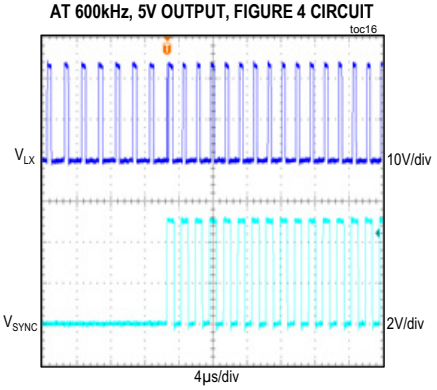
3.3V OUTPUT, PWM MODE, FIGURE 5 CIRCUIT (LOAD CURRENT STEPPED FROM NO LOAD TO 0.75A)



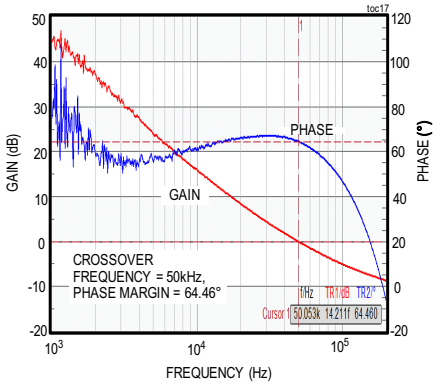
OVERLOAD PROTECTION 5V OUTPUT, FIGURE 4 CIRCUIT



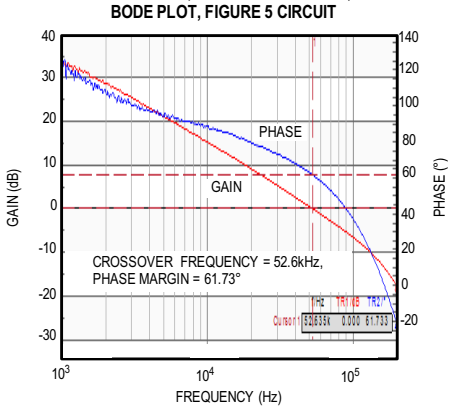
APPLICATION OF EXTERNAL CLOCK AT 600kHz, 5V OUTPUT, FIGURE 4 CIRCUIT



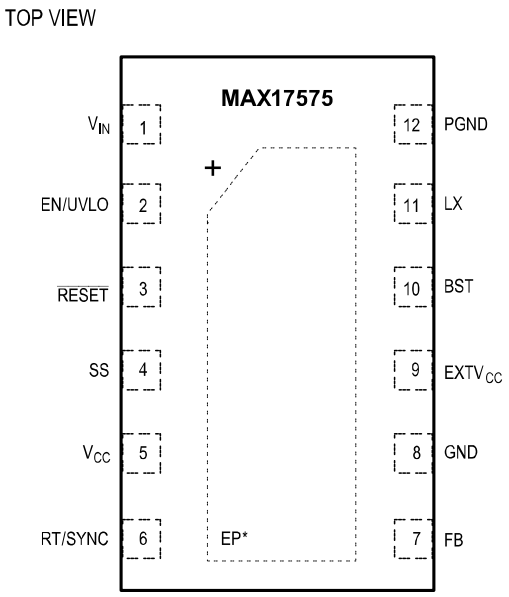
5V OUTPUT, 1.5A LOAD CURRENT, BODE PLOT, FIGURE 4 CIRCUIT



3.3V OUTPUT, 1.5A LOAD CURRENT, BODE PLOT, FIGURE 5 CIRCUIT



Pin Configuration



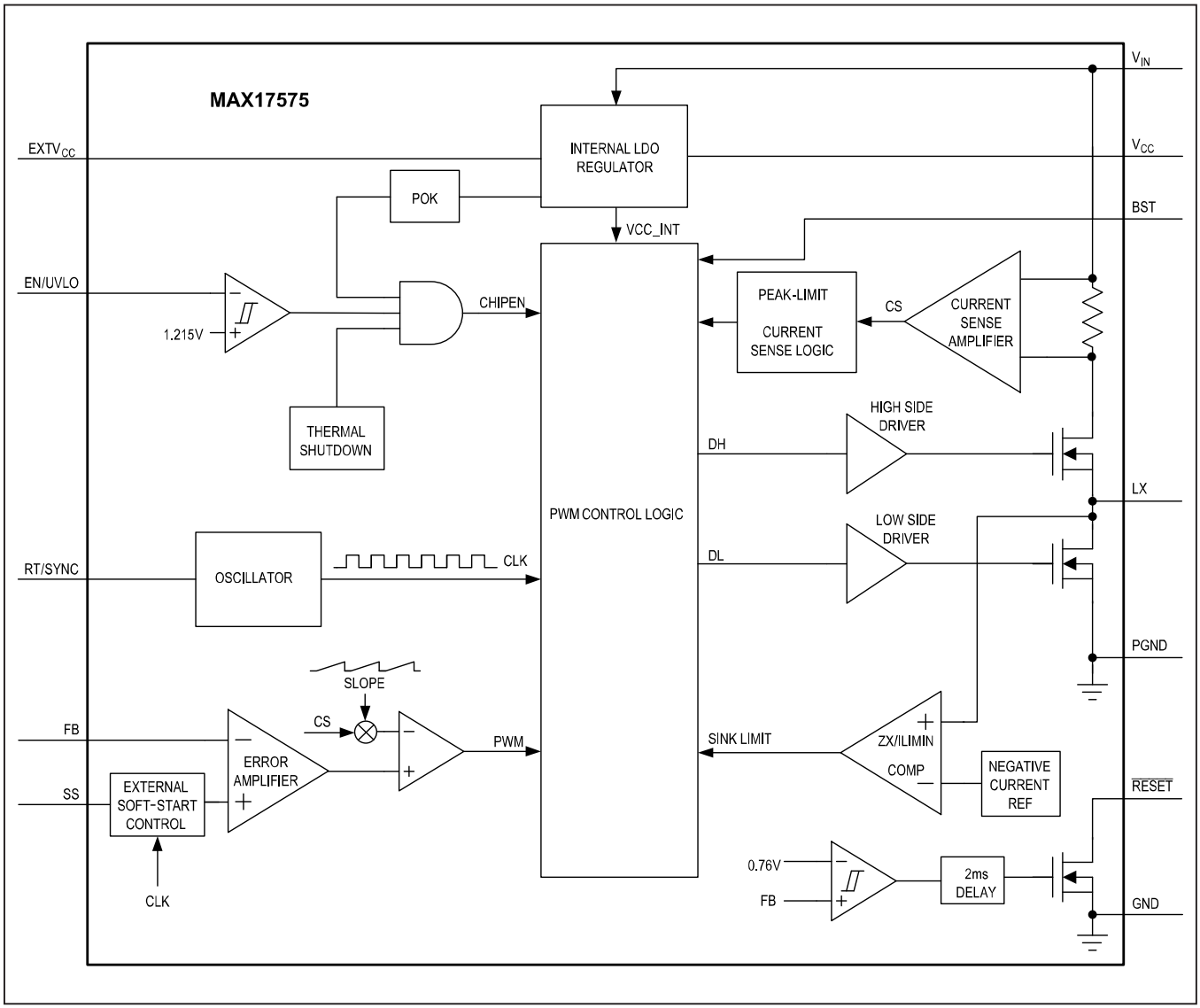
Pin Description

PIN	NAME	FUNCTION
1	V_{IN}	Power Supply Input. The input supply range is from 4.5V to 60V.
2	EN/UVLO	Enable/Undervoltage Lockout Input. Drive EN/UVLO high to enable the output voltage. Connect to the centre of the resistive divider between V_{IN} and GND to set the input voltage (undervoltage threshold) at which the device turns on. Pull up to V_{IN} for always-on.
3	$\overline{RESET}$	Open-Drain $\overline{RESET}$ Output. The $\overline{RESET}$ output is driven low if FB drops below 92% of its set value. $\overline{RESET}$ goes high 1024 clock cycles after FB rises above 95% of its set value. $\overline{RESET}$ is valid when the device is enabled and V_{IN} is above 4.5V.
4	SS	Soft-Start Input. Connect a capacitor from SS to GND to set the soft-start time.
5	V_{CC}	5V LDO Output. Bypass V_{CC} with 4.7µF/0805/10V/X7R ceramic capacitance to PGND.
6	RT/SYNC	Oscillator Timing Resistor Input. Connect a resistor from RT/SYNC to GND to program the switching frequency from 400kHz to 2.2MHz. See the Switching Frequency (RT/SYNC) section for details. An external pulse can be applied to RT/SYNC through a coupling capacitor to synchronize the internal clock to the external pulse frequency. See the *External Synchronization* section for details.
7	FB	Feedback Input. Connect FB to the center of the resistive divider between output voltage and GND.
8	GND	Analog Ground.
9	$EXTV_{CC}$	External Power-Supply Input for the Internal LDO. Applying a voltage between 4.84V and 24V at the $EXTV_{CC}$ pin will bypass the internal LDO and improve efficiency.

Pin Description (continued)

10	BST	Boost Flying Capacitor. Connect a 0.1µF ceramic capacitor between BST and LX.
11	LX	Switching Node. Connect LX to the switching side of the inductor. LX is high impedance when the device is in shutdown mode.
12	PGND	Power Ground. Connect PGND externally to the power ground plane. Connect GND and PGND pins together at the ground return path of the V_{CC} bypass capacitor.
—	EP	Exposed Pad. Connect to the GND pin of the IC. Connect to a large copper plane below the IC to improve heat dissipation capability.

Functional (or Block) Diagram



Detailed Description

The MAX17575 high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operates over a 4.5V to 60V input. The converter can deliver up to 1.5A and generates output voltages from 0.9V up to 0.9 x V_{IN}. The feedback (FB) voltage is accurate to within ±1.2% over -40°C to +125°C.

The device features a peak-current-mode control architecture. An internal transconductance error amplifier produces an integrated error voltage at an internal node that sets the duty cycle using a PWM comparator, a high-side current-sense amplifier, and a slope-compensation generator. At each rising edge of the clock, the high-side MOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached, or the peak current limit is detected. During the high-side MOSFET's on-time, the inductor current ramps up. During the second-half of the switching cycle, the high-side MOSFET turns off and the low-side MOSFET turns on. The inductor releases the stored energy as its current ramps down and provides current to the output.

The device features a RT/SYNC pin to program the switching frequency and to synchronize to an external clock. The device integrates adjustable-input, undervoltage-lockout, adjustable soft-start, open-drain $\overline{RESET}$, and auxiliary bootstrap LDO.

Linear Regulator (V_{CC})

The device has two internal (low-dropout) regulators (LDOs) which powers V_{CC}. One LDO is powered from VIN and the other LDO is powered from $EXTV_{CC}$ ($EXTV_{CC}$ LDO). Only one of the two LDOs is in operation at a time, depending on the voltage levels present at $EXTV_{CC}$. If $EXTV_{CC}$ voltage is greater than 4.7V (typ), V_{CC} is powered from $EXTV_{CC}$. If $EXTV_{CC}$ is lower than 4.7V (typ), V_{CC} is powered from V_{IN}. Powering V_{CC} from $EXTV_{CC}$ increases efficiency at higher input voltages. $EXTV_{CC}$ voltage should not exceed 24V.

Typical V_{CC} output voltage is 5V. Bypass V_{CC} to PGND with a 4.7µF low-ESR ceramic capacitor. V_{CC} powers the internal blocks and the low-side MOSFET driver and recharges the external bootstrap capacitor. Both LDO can source up to 60mA (typ). The MAX17575 employs an undervoltage-lockout circuit that forces both the regulators off when V_{CC} falls below 3.8V (typ). The regulators can be immediately enabled again when V_{CC} is higher than 4.2V. The 400mV UVLO hysteresis prevents chattering on power-up/power-down.

In applications where the buck converter output is connected to the $EXTV_{CC}$ pin, if the output is shorted to ground, then transfer from $EXTV_{CC}$ LDO to the internal LDO happens seamlessly without any impact on the normal functionality.

Switching Frequency Selection and External Frequency Synchronization

The switching frequency of the MAX17575 can be programmed from 400kHz to 2.2MHz by using a resistor connected from the RT/SYNC pin to GND. When no resistor is used, the frequency is programmed to 490kHz. The switching frequency (f_{SW}) is related to the resistor connected at the RT pin (R_{RT}) by the following equation:

$$R_{RT} = \frac{21 \times 10^3}{f_{SW}} - 1.7$$

where R_{RT} is in kΩ and f_{SW} is in kHz. See Table 1 for RT resistor values for a few common switching frequencies.

The RT/SYNC pin can be used to synchronize the device's internal oscillator to an external system clock. A resistor must be connected from the RT/SYNC pin to GND to be able to synchronize the MAX17575 to an external clock. The external clock should be coupled to the RT/SYNC pin through a network, as shown in Figure 1. When an external clock is applied to MODE/SYNC pin, the internal oscillator frequency changes to external clock frequency (from original frequency based on RT setting) after detecting 16 external clock edges. The external clock logic-high level should be higher than 2.1V, logic-low level lower than 0.8V and the pulse width of the external clock should be more than 50ns. The RT resistor should be selected to set the switching frequency at 10% lower than the external clock frequency.

Table 1. Switching Frequency vs. RT Resistor

SWITCHING FREQUENCY (kHz)	RT RESISTOR (kΩ)
400	51.1
500	OPEN
1000	19.1
2200	8.06

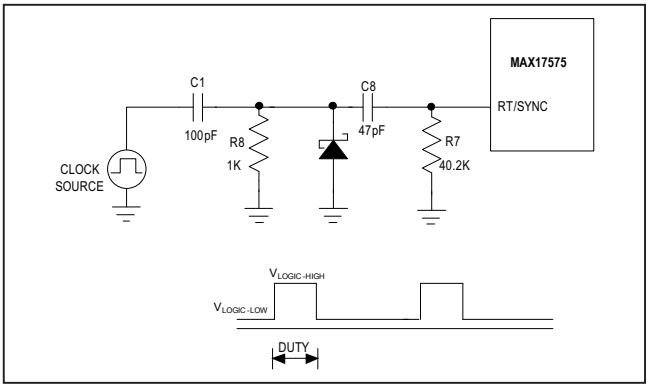


Figure 1. External Clock Synchronization

Operating Input-Voltage Range

The minimum and maximum operating input voltages for a given output voltage should be calculated as follows:

$$V_{IN(MIN)} = \frac{V_{OUT} + (I_{OUT(MAX)} \times (R_{DCR} + R_{DS-ONL}))}{D_{MAX}} + (I_{OUT(MAX)} \times (R_{DS-ONH} - R_{DS-ONL}))$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{f_{SW(MAX)} \times t_{ON(MIN)}}$$

Where V_{OUT} is the steady-state output voltage, $I_{OUT\ (MAX)}$ is the maximum load current, R_{DCR} is the DC resistance of the inductor, $f_{SW(MAX)}$ is the maximum switching frequency, $t_{OFF(MAX)}$ is the worst-case minimum switch off-time (160ns) and t_{ON-MIN} is the worst-case minimum switch on-time (80ns).

Overcurrent Protection

The device is provided with a robust overcurrent protection scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET whenever the high-side switch current exceeds an internal limit of 2.45A (typ). A runaway current limit on the high-side switch current at 2.75A (typ) protects the device under high input voltage, short-circuit conditions when there is insufficient output voltage available to restore the inductor current that was built up during the on period of the step-down converter. One occurrence of runaway current limit triggers a hiccup mode. In addition, if, due to a fault condition, feedback voltage drops to 0.58V (typ) any time after soft-start is complete, hiccup mode is triggered. In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 32,768 clock cycles. Once the hiccup timeout period expires, soft-start is attempted again. Note that when soft-start is attempted under an overload condition, if the feedback voltage does not exceed 0.58V, the device switches at half the programmed switching frequency. Hiccup mode of operation ensures low power dissipation under output short-circuit conditions.

$\overline{\text{RESET}}$ Output

The device includes a $\overline{\text{RESET}}$ comparator to monitor the output voltage. The open-drain $\overline{\text{RESET}}$ output requires an external pullup resistor. $\overline{\text{RESET}}$ goes high (high impedance) 1024 switching cycles after the regulator output increases above 95% of the designed nominal regulated voltage. $\overline{\text{RESET}}$ goes low when the regulator output voltage drops to below 92% of the nominal regulated voltage. $\overline{\text{RESET}}$ also goes low during thermal shutdown.

Prebiased Output

When the device starts into a prebiased output, both the high-side and low-side switches are turned off so that the converter does not sink current from the output. High-side and low-side switches do not start switching until the PWM comparator commands the first PWM pulse. The output voltage is then smoothly ramped up to the target value in alignment with the internal reference.

Thermal Shutdown Protection

Thermal shutdown protection limits total power dissipation in the device. When the junction temperature of the device exceeds +165°C, an on-chip thermal sensor shuts down the device, allowing the device to cool. The thermal sensor turns the device on again after the junction temperature cools by 10°C. Soft-start resets during thermal shutdown. Carefully evaluate the total power dissipation (see the *Power Dissipation* section) to avoid unwanted triggering of the thermal shutdown protection in normal operation.

Typical Application Circuit

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor RMS current (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where, $I_{OUT(MAX)}$ is the maximum load current. I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = 2 x V_{OUT}), so $I_{RMS(MAX)} = I_{OUT(MAX)}/2$.

Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times (1 - D)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where D = V_{OUT}/V_{IN} is the duty ratio of the controller, f_{SW} is the switching frequency, ΔV_{IN} is the allowable input voltage ripple, and η is the efficiency.

In applications where the source is located distant from the device input, an electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}) and DC resistance (R_{DCR}). The switching frequency and output voltage determine the inductor value as follows:

$$L = \frac{2 \times V_{OUT}}{f_{SW}}$$

Where V_{OUT} and f_{SW} are nominal values and f_{SW} is in Hz. Select an inductor whose value is nearest to the value calculated by the previous formula.

Select a low-loss inductor closest to the calculated value with acceptable dimensions and having the lowest possible DC resistance. The saturation current rating (I_{SAT}) of the inductor must be high enough to ensure that saturation can occur only above the peak current-limit value.

Output Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. The output capacitors are usually sized to support a step load of 50% of the maximum output current in the application, so the output voltage deviation is contained to 3% of the output voltage change. The minimum required output capacitance can be calculated as follows:

$$C_{OUT} = \frac{60}{V_{OUT}}$$

Where C_{OUT} is in µF. Derating of ceramic capacitors with DC-voltage must be considered while selecting the output capacitor. Derating curves are available from all major ceramic capacitor vendors.

Soft-Start Capacitor Selection

The device implements adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to GND programs the soft-start time. The selected output capacitance (C_{SEL}) and the output voltage (V_{OUT}) determine the minimum required soft-start capacitor as follows:

$$C_{SS} \geq 56 \times 10^{-6} \times C_{SEL} \times V_{OUT}$$

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$t_{SS} = \frac{C_{SS}}{5.55 \times 10^{-6}}$$

For example, to program a 2ms soft-start time, a 12nF capacitor should be connected from the SS pin to GND.

Adjusting Output Voltage

Set the output voltage with a resistive voltage-divider connected from the positive terminal of the output capacitor (V_{OUT}) to SGND (see Figure 2). Connect the center node of the divider to the FB pin. Use the following procedure to choose the resistive voltage-divider values:

Calculate resistor R4 from the output to the FB pin as follows:

$$R4 = \frac{1850}{C_{OUT\_SEL}}$$

Where C_{OUT_SEL} (in µF) is the actual derated value of the output capacitance used and R4 is in kΩ. The minimum allowable value of R4 is (5.6 x V_{OUT}), where R4 is in kΩ. If the value of R4 calculated using the above equation is less than (5.6 x V_{OUT}), increase the value of R4 to at least (5.6 x V_{OUT}).

$$R5 = \frac{R4 \times 0.9}{(V_{OUT} - 0.9)}$$

R5 is in kΩ.

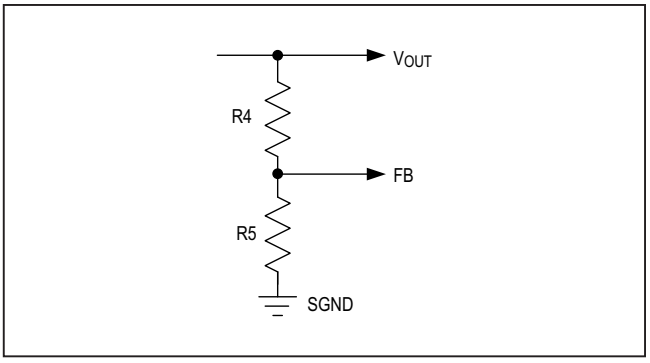


Figure 2. Adjusting Output Voltage

Setting the Undervoltage Lockout Level

The device offers an adjustable input undervoltage-lockout level. Set the voltage at which the device turns on with a resistive voltage-divider connected from V_{IN} to SGND (Figure 3). Connect the center node of the divider to EN/UVLO. Choose R1 to be 3.3MΩ and then calculate R2 as follows:

$$R2 = \frac{1.215 \times R1}{(V_{INU} - 1.215)}$$

where V_{INU} is the voltage at which the device is required to turn on. Ensure that V_{INU} is higher than 0.8 x V_{OUT}.

If the EN/UVLO pin is driven from an external signal source, a series resistance of minimum 1kΩ is recommended to be placed between the signal source output and the EN/UVLO pin, to reduce voltage ringing on the line.

Power Dissipation

At a particular operating condition, the power losses that lead to temperature rise of the part are estimated as follows:

$$P_{LOSS} = (P_{OUT} \times (\frac{1}{\eta} - 1)) - \left(I_{OUT}{}^2 \times R_{DCR}\right)$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

Where P_{OUT} is the output power, η is the efficiency of the converter and R_{DCR} is the DC resistance of the inductor (see the *Typical Operating Characteristics* for more information on efficiency at typical operating conditions).

For a typical multilayer board, the thermal performance metrics for the package are given below:

$$\theta_{JA} = 41°C / W$$

$$\theta_{JC} = 8.5°C / W$$

The junction temperature of the device can be estimated at any given maximum ambient temperature (T_{A_MAX}) from the following equation:

$$T_{J\_MAX} = T_{A\_MAX} + (\theta_{JA} \times P_{LOSS})$$

If the application has a thermal-management system that ensures that the exposed pad of the device is maintained at a given temperature (T_{EP_MAX}) by using proper heat sinks, the junction temperature of the device can be estimated at ayn given maximum ambient temperature as:

$$T_{J\_MAX} = T_{EP\_MAX} + (\theta_{JC} \times P_{LOSS})$$

Junction temperatures greater than +125°C degrades operating lifetimes.

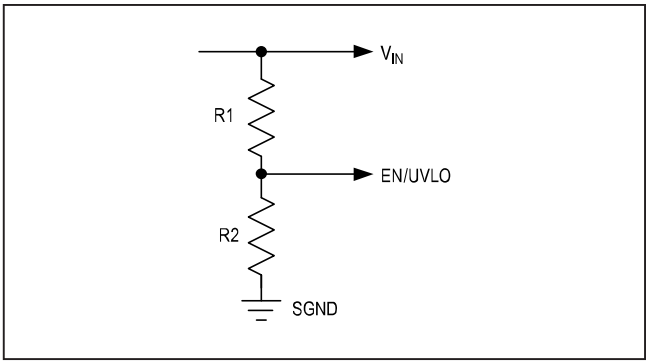


Figure 3. Setting the Input Undervoltage Lockout

PCB Layout Guidelines

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents. Since inductance of a current carrying loop is proportional to the area enclosed by the loop, if the loop area is made very small, inductance is reduced. Additionally, small-current loop areas reduce radiated EMI.

A ceramic input filter capacitor should be placed close to the V_{IN} pins of the IC. This eliminates as much trace inductance effects as possible and gives the IC a cleaner voltage supply. A bypass capacitor for the V_{CC} pin also should be placed close to the pin to reduce effects of trace impedance.

When routing the circuitry around the IC, the analog small-signal ground and the power ground for switching currents must be kept separate. They should be connected together at a point where switching activity is at a minimum, typically the return terminal of the V_{CC} bypass capacitor. This helps keep the analog ground quiet. The ground plane should be kept continuous/unbroken as far as possible. No trace carrying high switching current should be placed directly over any ground plane discontinuity.

PCB layout also affects the thermal performance of the design. A number of thermal vias that connect to a large ground plane should be provided under the exposed pad of the part, for efficient heat dissipation.

For a sample layout that ensures first pass success, refer to the MAX17575 evaluation kit layout available at www.maximintegrated.com.

Typical Application Circuit

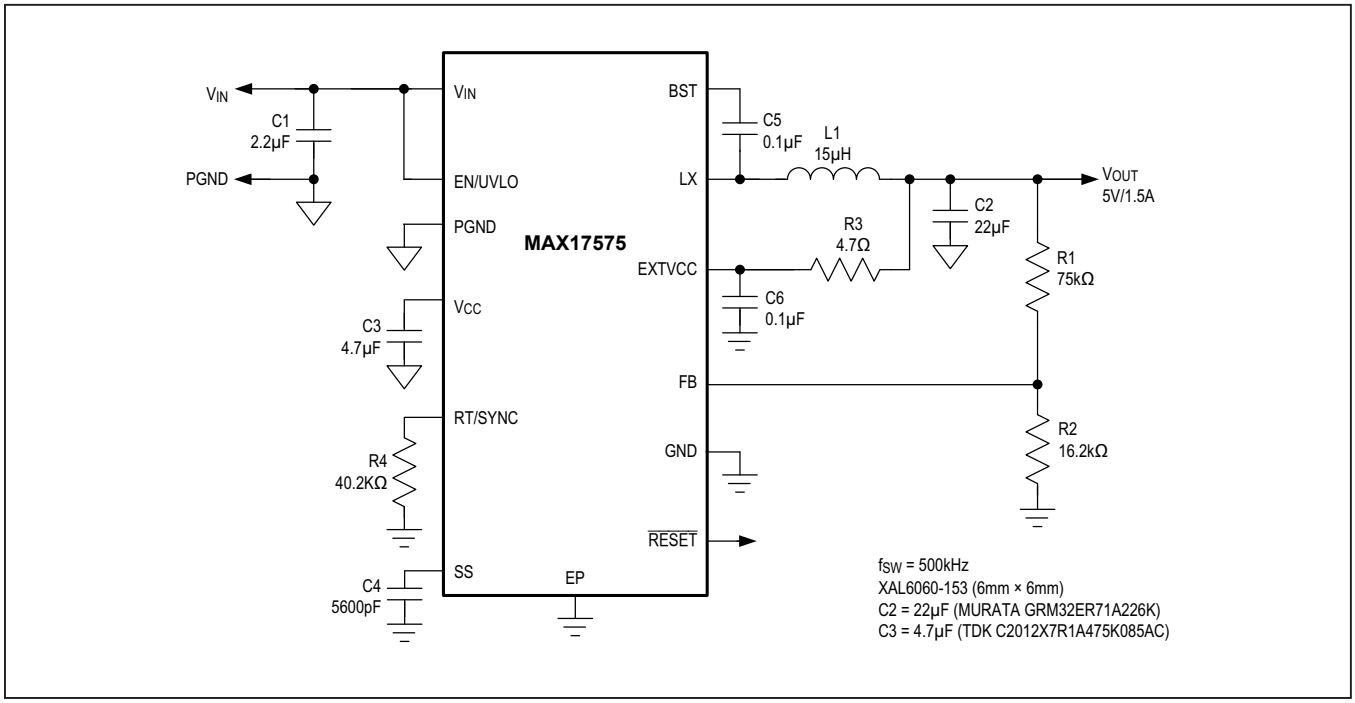


Figure 4. Typical Application Circuit for 5V Output

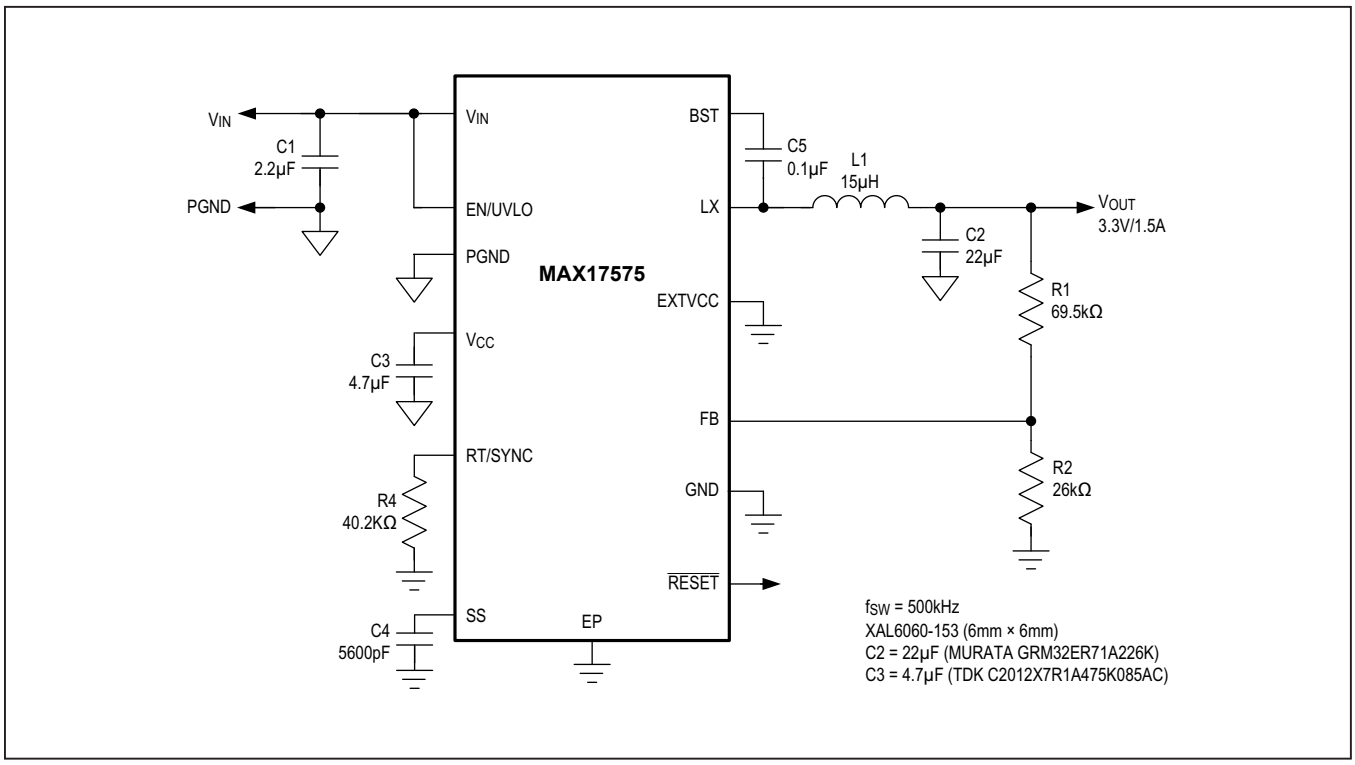


Figure 5. Typical Application Circuit for 3.3V Output

Ordering Information

PART	PIN-PACKAGE	PACKAGE-SIZE
MAX17575ATC+	12-TDFN EP*	3mm x 3mm

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/17	Initial release	—
1	6/17	Updated global conditions for the *Electrical Characteristics* table, *Typical Operating Characteristics*, *Pin Description* table 5V LDO Output (V_{CC} pin) Function, and the *Linear Regulator (V_{CC})* section. Updated Equation in the *Operating Input-Voltage Range* section, limits in the *Overcurrent Protection* section, and *Typical Application Circuits*.	1–8, 10–11, 14

